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The S-LINK 64 bit extension specification: S-LINK64

Attila Racz, Robert McLaren & Erik van der Bij
EP Division, CERN.

S-LINK64 specifies the extension to S-LINK to achieve higher throughput (up to 800 MByte/sec) required by some modern Data Acquisition Systems.

This document complements the original S-LINK specs; users are assumed to be familiar with S-LINK.

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1.0 Scope

1.1 S-LINK extension specification

The main motivation of this extension is the need for higher throughput. This document does not replace the original S-LINK specification. For complete information on S-LINK, please refer to the specification to be found on:

http://hsi.web.cern.ch/HSI/s-link/

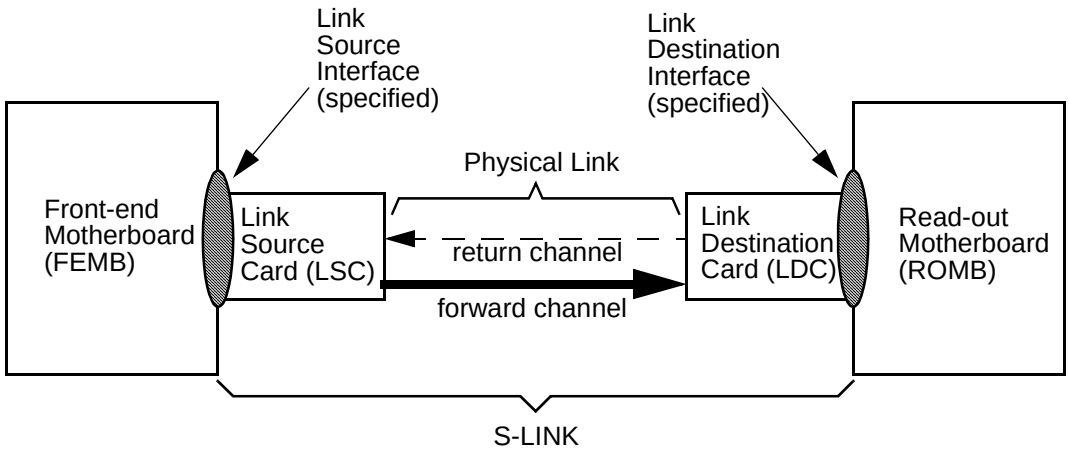
1.2 S-LINK principle

S-LINK is a Simple Link Interface which can be used to connect any layer of front-end electronics to the next layer of read-out. An S-LINK is a link complying to this specification and can be thought of as a virtual ribbon cable, moving data or control words from one point to another. In addition to simple data movement, S-LINK includes the following features;

- Error detection.
- Return channel for flow control and for return line signals *(duplex version only)*.
- Self-test function.

The S-LINK specification describes the interface between the Front-end Motherboard (FEMB) and the Link Source Card (LSC) and the interface between the Link Destination Card (LDC) and the Read-out Motherboard (ROMB). It does *not* describe the physical link itself. This concept is shown in Figure 1.

FIGURE 1. The S-LINK concept



1.3 Implementation Guide

This specification is written from the point-of-view of the S-LINK user (that is, the designer of the FEMB or ROMB). For the designer of an S-LINK, an implementation guide is available which includes advice on how to implement the various features of the S-LINK.

2.0 Features

Whereas S-LINK can be simplex or duplex, S-LINK64 is not intended to have a simplex implementation.

2.1 Features common to S-LINK and S-LINK64

1. **Control/Data bit:** All words transmitted are accompanied by an additional bit which enables the user to mark any word and thus identify the word with a private meaning (e.g. *block_address, event_header, end_of_block* etc.).
2. **Error Reporting:** An S-LINK64 detects transmission errors and reports these using the LDERR# line. In addition, the *data error* LED is illuminated and held until reset.
3. **Test Function:** The LSC and LDC can be switched to a test mode where the LSC transmits a fixed pattern which the LDC verifies. If any data errors are detected, the LDC illuminates the data error LED. The test pattern can be transferred to the ROMB by the LDC if desired.
4. **Reset Function:** A hard reset function is provided on both the LSC and the LDC.
5. **Flow Control:** When data cannot be accepted by the LSC, LFF# is asserted. This signal indicates to the FEMB that the data transfer must be interrupted: subsequent data may be lost. LFF# is asserted under one of the two following conditions:
   - The ROMB asserts the signal UXOFF# at the LDC which causes it to transmit an *XOFF* code to the LSC. In turn, the LSC asserts LFF#. When UXOFF# is de-asserted, an *XON* code is transmitted to the LSC which in turn de-asserts LFF#
   - The LSC itself asserts LFF# when the incoming data stream overloads the physical link bandwidth.
6. **Return Lines:** The state of four lines is continually sampled at the LDC, transmitted back to the LSC and presented to the FEMB. To the user, this looks like four wires running back from the LDC to the LSC.

2.2 Features found only with S-LINK64

The 64-bit version provides additional features for the user via an extension connector:

1. **64-bit Data Width:** an S-LINK64 shall be built with a data width of 64-bit.
2. **Data transfer interruption:** after LFF# is asserted, the data transfer must be effectively interrupted within 16 clocks (2 clocks when S-LINK). Subsequent data are ignored.
3. **Local JTAG port:** the Test Access Port allows local testing/configuration of the connected S-LINK64 link card.
4. Additional power supplies: power pins are provided to allow easy usage of components requiring 3.3V and 2.5V.

2.3 Compatibility

There is no physical compatibility between S-LINK and S-LINK64 modules. The compatibility is at the protocol level only. However, as the S-LINK64 specific signals are located on a separate connector and no changes affect the other connector, one can easily design a FEMB or a ROMB that can adapt to both board types.

2.4 Extension connector

The extension connector houses 32 additional data lines to reach a 64-bit data path, JTAG Test Access Port, special functions lines, and additional power supplies pins. No other control or status signals have been added on the extension connector in order to maintain the philosophy of S-LINK.

3.0 Definitions

3.1 Hardware Components

An S-LINK64 is composed of two components: The *Link Source Card* (LSC) which is mounted on the user's front-end electronics (called the *Front-end Motherboard:* FEMB) and is the transmitter of data. The *Link Destination Card* (LDC) is mounted on the user's data collection electronics (called the *Read-out Motherboard:* ROMB) and is the receiver of data. When the LSC and LDC are referred to together, they are called the S-LINK64.

3.2 Terminology

To avoid confusion, certain keywords have special meanings:

- *Shall* indicates a mandatory requirement. The instruction given has to be followed to conform to the specification. Failure to do so will lead to a non-conforming design which may not work.
- *Should* means that the designer does not need to follow the instruction given and can treat it as a recommendation.
- *May* means that an option is available.
- *Transfer* relates to data crossing the interface between the FEMB and the LSC or the interface between the LDC and the ROMB.
- *Transmit* relates to data travelling along the physical layer between the LSC and the LDC.

These keywords are only used in these contexts.

3.3 Signal Names

All signal names are printed in capital letters. Signals are defined as inputs or outputs to or from the S-LINK64 as follows:

- Signals which are generated by the user are prefixed with the letter "U", e.g. UD0, UWEN# etc. These signals are inputs to the S-LINK64.
- Signals which are generated by the S-LINK64 are prefixed with the letter "L", e.g. LD0, LWEN# etc. These signals are outputs from the S-LINK64.
- All signals which have an active state are **active when low** and **inactive when high**. Such signal names are terminated with a "#" character. *Low* and *High* refer to the signal levels which are defined electrically in Table 6.

Note that this convention applies in the same way at each end of the S-LINK64, i.e. at the LSC and LDC.

3.4 Signal Line Functions

The extension connector signal lines for the LSC are described in Table 1. The extension connector signal lines for the LDC are described in Table 2.

The description of the original S-LINK signal line can be found in the S-LINK Specification.

TABLE 1. Signal Description for the LSC extension connector

Pin Symbol	Pin Name	I/O	Description
UD[63..32]	User Data input lines	Input to S-LINK64	Data on these lines is transferred to the LSC on a low-to-high transition of UCLK when UWEN is low. Synchronous with UCLK.
UJCLK	User JTAG Clock line	Input to S-LINK64	Local JTAG clock (optional). Pull up on the FEMB to 3.3V with 10 KOhm.
UJTMS	User JTAG Test Mode Setup line	Input to S-LINK64	Local JTAG test mode setup (optional). Pull up on the FEMB to 3.3V with 10 KOhm.
UJTDI	User JTAG Test Data In line	Input to S-LINK64	Local JTAG test data in (optional). Synchronous with UJCLK. If not implemented on the FEMB, pullup to 3.3V with 10K Ohm. If not implemented on the LSC, UJTDI shall be connected to LJTDO.
LJTDO	Link JTAG Test Data Out line	Output from S-LINK64	Local JTAG test data out (optional). Synchronous with UJCLK. If not implemented on the FEMB, pullup to 3.3V with 10K Ohm. If not implemented on the LSC, LJTDO shall be connected to UJTDI.
USF[3..0]	Special functions input lines	Input to S-LINK64	The usage of these lines is dependent on the physical implementation of the link cards. (see Table 5)
LSF[3..0]	Special functions output lines	Output from S-LINK64	The usage of these lines is dependent on the physical implementation of the link cards. (see Table 5)

TABLE 2. Signal Description for the LDC extension connector

Pin Symbol	Pin Name	I/O	Description
LD[63..32]	Link Data output lines	Output from S-LINK64	Data present on these lines may be latched on the low-to-high transition of LCLK when LWEN# is low. Synchronous with LCLK.
UJCLK	User JTAG Clock line	Input to S-LINK64	Local JTAG clock (optional). Pull up on the ROMB to 3.3V with 10 KOhm.
UJTMS	User JTAG Test Mode Setup line	Input to S-LINK64	Local JTAG test mode setup (optional). Pull up on the ROMB to 3.3V with 10 KOhm.
UJTDI	User JTAG Test Data In line	Input to S-LINK64	Local JTAG test data in (optional). Synchronous with UJCLK. If not implemented on the ROMB, pullup to 3.3V with 10K Ohm. If not implemented on the LDC, UJTDI shall be connected to LJTDO.
LJTDO	Link JTAG Test Data Out line	Output from S-LINK64	Local JTAG test data out (optional). Synchronous with UJCLK. If not implemented on the ROMB, pullup to 3.3V with 10K Ohm. If not implemented on the LDC, LJTDO shall be connected to UJTDI.
USF[3..0]	Special functions input lines	Input to S-LINK64	The usage of these lines is dependent on the physical implementation of the link cards. (see Table 5)
LSF[3..0]	Special functions output lines	Output from S-LINK64	The usage of these lines is dependent on the physical implementation of the link cards. (see Table 5)

4.0 S-LINK64 Usage Instructions

4.1 Overview

This section describes in detail how the S-LINK64 can be used and how each feature works.

4.2 Maximum Clock Frequency and Data Transfer Rate

An S-LINK64 link card *shall* have a maximum clock frequency. This is defined as:

- 100 MHz

The clock pins are LCLK and UCLK and are located on the original S-LINK connector. These pins are not on the extension connector.

Note that the Data Transfer Rate depends on the physical implementation and the protocol used on the S-LINK64. The Data Sheet which accompanies each S-LINK64 *shall* detail the Data Transfer Rate. The values of timing parameters are given in Table 3. Timing parameters which relate to the LSC are suffixed with a -S while those which relate to the LDC are suffixed with a -D.

TABLE 3. Timing Parameters

Symbol	Description	Min	Max	Units
t_{DS-S}, t_{DS-D}	Data Set-up time	4.5		ns
t_{DH-S}, t_{DH-D}	Data Hold time	0.5		ns
t_{ENS-S}, t_{ENS-D}	Enable Set-up time	4.5		ns
t_{ENH-S}, t_{ENH-D}	Enable Hold time	0.5		ns
t_{WFF-S}	Write Clock to Full Flag		5.5	ns
t_{CLK-S}, t_{CLK-D}	Clock Cycle time	10		ns
$t_{CH-S,}$ t_{CH-D}	Clock High time	4.0		ns
$t_{CL-S,}$ t_{CL-D}	Clock Low time	4.0		ns

4.3 Data width

The combination UDW1=’1’ and UDW0=’1’ is now assigned to 64-bit data width. This was a reserved combination for S-LINK.

TABLE 4. Data Width Selection Codes

Data Width	UDW1	UDW0
32-bit	0	0
16-bit	0	1
8-bit	1	0
64-bit	1	1

4.4 Signal usage

4.4.1 Data lines UD[63..32] and LD[63..32]

The additional data lines fully behave like the original S-LINK data lines.

4.4.2 Link Full flag

LFF# behaves differently compaired to original S-LINK control line. (see 2.2)

4.4.3 JTAG Test Access Port (TAP)

The TAP is provided for local test/configuration of the S-LINK64 link card mounted on a ROMB or a FEMB. It shall not be used to transfer data over the link itself. For detailed usage of the JTAG pins, please refer to IEEE Std. 1149.1. The TAP on the motherboards as well as on the link cards is optional.

If not implemented on the FEMB or ROMB, UJCLK, UJTMS, UJTDI and LJTDO must be pulled-up to 3.3V with a 10 KOhm resistor.
If not implemented on the LSC or LDC, UJTDI shall connect to LJTDO.

4.4.4 Special function lines USF[3..0] and LSF[3..0]

The special function lines may be used for functions specific to a link implementation. To guarantee interoperability, the values other than 0's are not recommanded.

TABLE 5. Special functions description

Pin Name	Value	Description
USF[3..0]	"0000"	Standard 64-bit transfer
LSF[3..0]	"0000"	Standard 64 bit transfer

Depending on the link implementation, other values may exist: they will be documented in the link specification.

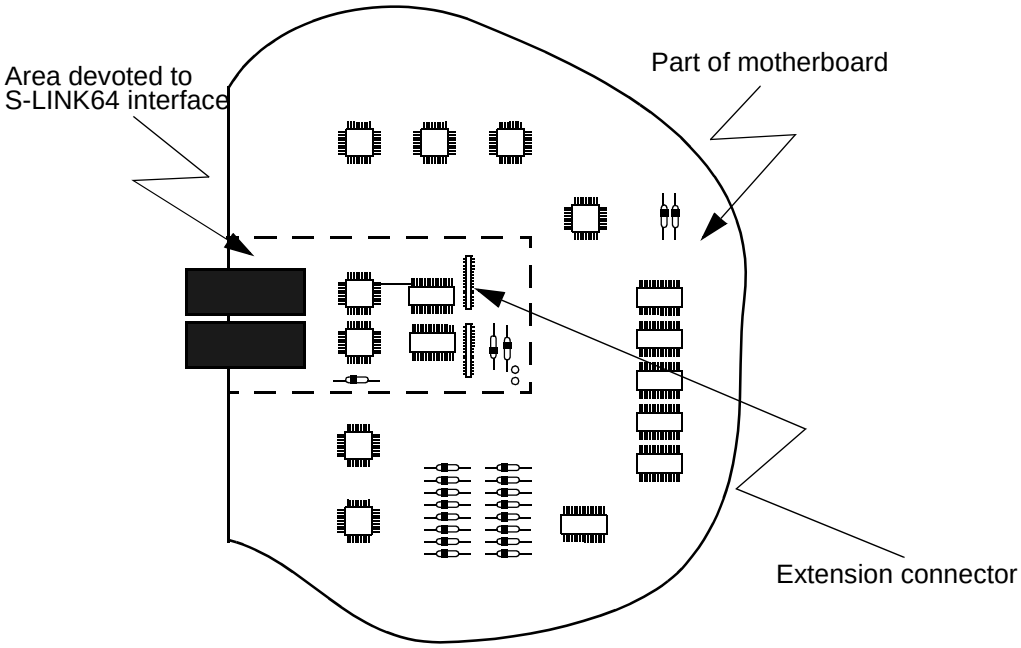
Users wishing to define new functions shall inform the authors of the present document.

5.0 Physical description

5.1 Example Implementations

This specification is concerned with describing an *interface* between the user's motherboards and the S-LINK64. The implementer of the S-LINK64 is free to use any physical arrangement desired. For example, one implementation could be to integrate the S-LINK64 interface into the motherboard as shown in Figure 2.

FIGURE 2. An S-LINK64 interface integrated into a motherboard



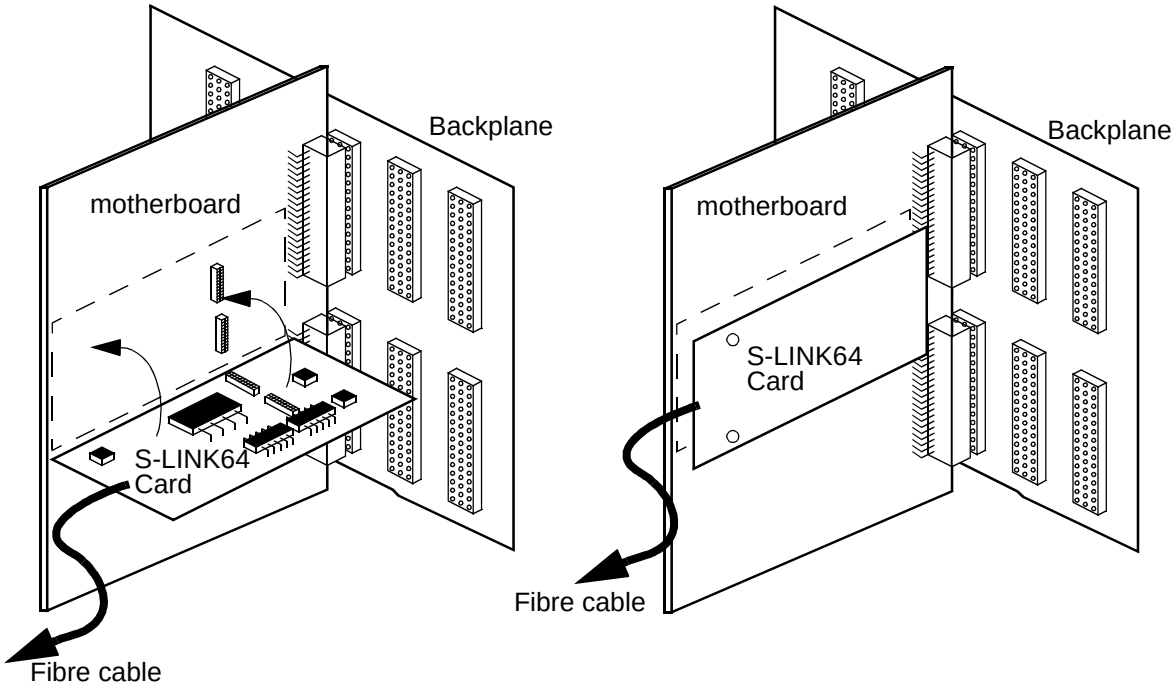
Alternatively, some users may wish to have separate S-LINK64 cards which are then mounted on the motherboard. If such users have no preferred physical arrangement, it is *recommended* that they construct the S-LINK64 cards according to the description given in Section 5.2. S-LINK64 cards have the same physical size as S-LINK cards with only the extension connector added.

An example of how such an implementation might appear is shown in Figure 3 which shows an S-LINK64 card mounted on a 6U VME motherboard.

5.2 Recommended Physical Arrangement

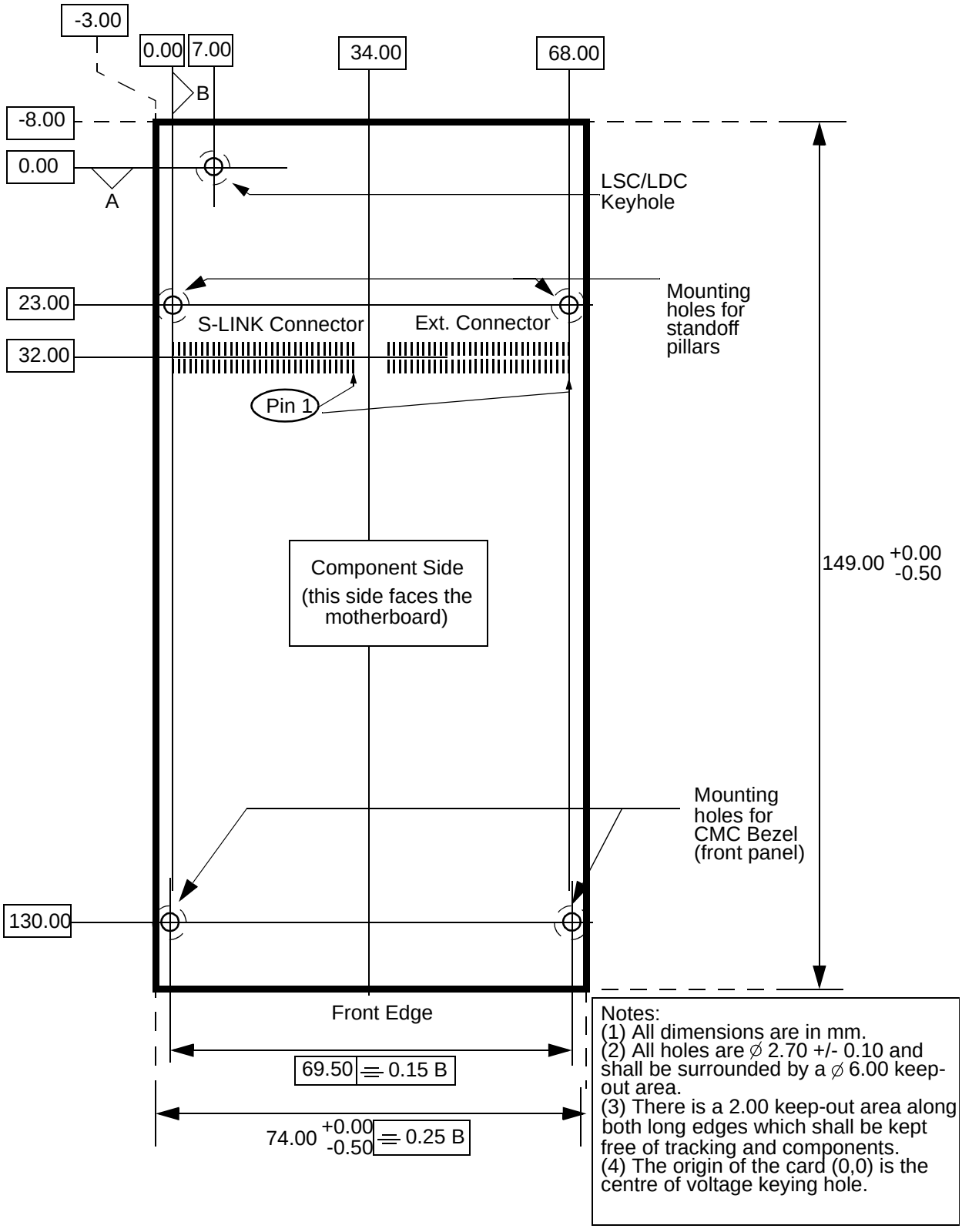
The S-LINK64 cards are based on single size Common Mezzanine Cards as defined in IEEE P1386/Draft 2.0 04-APR-1995, *Standard for a Common Mezzanine Card Family: CMC* (the CMC Standard).

FIGURE 3. A representation of how an S-LINK64 card is mounted on a 6U VME motherboard.



The physical shape of the S-LINK64 card *should* be as defined in Figure 4.

FIGURE 4. S-LINK64 card



6.0 Electrical description

6.1 Power Requirements

The S-LINK64 cards *shall* operate from positive supplies which *shall* be sourced directly from the motherboard. V_{cc} shall be +3.3 V and is housed on the original S-LINK connector. The extension connector houses additional +2.5 V power supplies (Vcc2.5).

The overall maximum power dissipation *shall* be 7.5 W.

On the FEMB or ROMB, Vcc2.5 shall provide 800 mA minimum and Vcc3.3 shall provide 2.3A minimum.
On the LSC or LDC, Vcc2.5 shall drain 800 mA maximum and Vcc3.3 shall drain 2.3A maximum.

FEMB/ROMB designers are invited to implement “confortable” safety margins regarding the power supplies as it is very likely that the first link card prototypes will exceed the above requirements.

The designer *shall* define on the Data Sheet the supply voltages required and the maximum power consumption.

6.2 Signal Levels

TABLE 6. DC Signalling Specifications

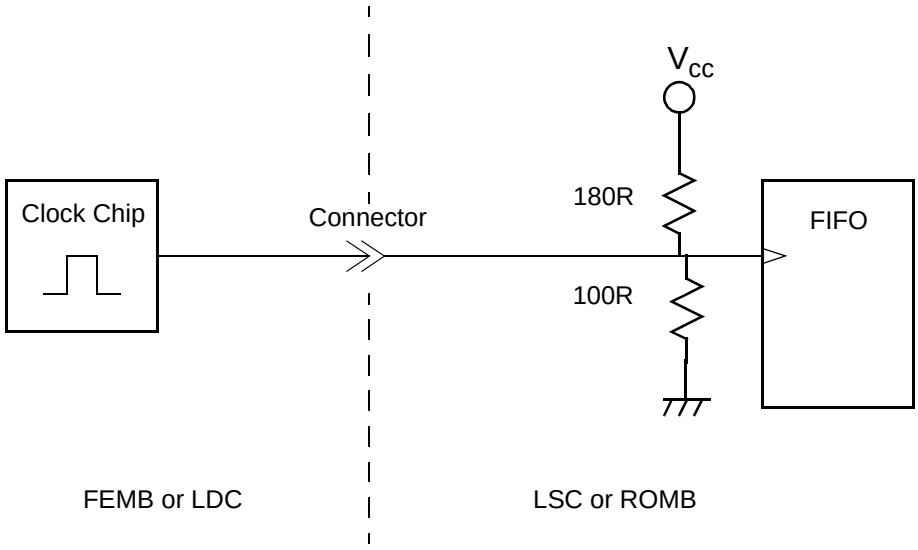
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	Volts
V_{IH}	Input high voltage level	$0.5V_{CC}$	V_{CC} + 0.5	Volts
V_{IL}	Input low voltage level	-0.5	$0.3V_{CC}$	Volts
V_{OH}	Output high voltage level	$0.9V_{CC}$ (I_{OL} = -500 µA)		Volts
V_{OL}	Output low voltage level		$0.1V_{CC}$ (I_{OL} = 1500 µA)	Volts

Note that link cards are not required to be “5 volts tolerant.”

6.3 Clock Signal Terminations

To ensure a clean clock signal, the designer of an LSC or a ROMB *should* terminate the incoming clock signals (UCLK and LCLK) from the FEMB and LDC respectively. An example of a termination resistance network which *may* be used is shown in Figure 5.

FIGURE 5. Example of a clock signal termination resistance network



7.0 Extension Connector Pinout Diagrams

The pinout diagram for the LSC is shown in Table 7. The pinout diagram for the LDC is shown in Table 8. Both these diagrams represent the actual footprint of the connector when viewed **onto the motherboard**.

TABLE 7. Pinout Diagram for the LSC extension connector (view onto the motherboard)

1	UJCLK	UJTMS	2
3	Reserved	UJTDI	4
5	USF3	UJTDO	6
7	USF2	GND	8
9	GND	Reserved	10
11	USF1	GND	12
13	GND	Reserved	14
15	USF0	GND	16
17	LSF3	LSF2	18
19	LSF1	LSF0	20
21	UD63	Vcc2.5	22
23	GND	UD62	24
25	UD61	UD60	26
27	UD59	GND	28
29	UD58	UD57	30
31	GND	UD56	32
33	UD55	UD54	34
35	UD53	GND	36
37	UD52	UD51	38
39	Vcc2.5	UD50	40
41	UD49	UD48	42
43	UD47	GND	44
45	UD46	UD45	46
47	GND	UD44	48
49	UD43	UD42	50
51	UD41	Vcc2.5	52
53	UD40	UD39	54
55	GND	UD38	56
57	UD37	UD36	58
59	UD35	GND	60
61	UD34	UD33	62
63	Vcc2.5	UD32	64

Reserved pins must be left unconnected.

TABLE 8. Pinout Diagram for the LDC extension connector (view onto the motherboard)

1	UJCLK	UJTMS	2
3	Reserved	UJTDI	4
5	USF3	UJTDO	6
7	USF2	GND	8
9	GND	Reserved	10
11	USF1	GND	12
13	GND	Reserved	14
15	USF0	GND	16
17	LSF3	LSF2	18
19	LSF1	LSF0	20
21	LD63	Vcc2.5	22
23	GND	LD62	24
25	LD61	LD60	26
27	LD59	GND	28
29	LD58	LD57	30
31	GND	LD56	32
33	LD55	LD54	34
35	LD53	GND	36
37	LD52	LD51	38
39	Vcc2.5	LD50	40
41	LD49	LD48	42
43	LD47	GND	44
45	LD46	LD45	46
47	GND	LD44	48
49	LD43	LD42	50
51	LD41	Vcc2.5	52
53	LD40	LD39	54
55	GND	LD38	56
57	LD37	LD36	58
59	LD35	GND	60
61	LD34	LD33	62
63	Vcc2.5	LD32	64

Reserved pins must be left unconnected.

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10.0 Revision History

- **December 11, 2000: First version released.**
- **August 4, 2003: When Link Full Flag asserted, up to 16 clocks are allowed before data loss**

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11.0 Glossary

CMC	Common Mezzanine Card
FEMB	Front-End Motherboard
LCLK	Link Clock
LCTRL#	Link Control bit
LD[63..0]	Link Data
LDC	Link Destination Card
LDERR#	Link Data Error
LDOWN#	Link Down
LFF#	Link Full Flag
LRL[3..0]	Link Return Line
LSC	Link Source Card
LSF[3..0]	Link Special function
LWEN#	Link Write Enable
ROMB	Read-Out Motherboard
UCLK	User Clock
UCTRL#	User Control bit
UD[63..0]	User Data
UDW	User Data Width
UJCLK	User JTAG clock
UJTMS	User JTAG Test Mode Setup
UJTDI	User JTAG Test Data In
UJTDO	User JTAG Test Data Out
UTDO#	User Test Data Out
URESET#	User Reset
URL[3..0]	User Return Line
USF[3..0]	User Special Function
UTEST#	User Test
UWEN#	User Write Enable
UXOFF#	User Xmit Off